Previous Doc Next Doc Go to Doc#
First Hit

Generate Collection

L50: Entry 1 of 1 File: JPAB Mar 13, 1989

DOCUMENT-IDENTIFIER: JP 01066578 A
TITLE: DELAY ANALYSIS SYSTEM OF LOGICAL CIRCUIT

Abstract Text (1):
PURPOSE: To easily judge the quality of a delay analytical result, by judging whether a path exceeding a delay time is the meaningless redundant path on a logical circuit according to a route activating method and removing the redundant path from a delay analytical result list.

Abstract Text (2):
CONSTITUTION: A logical circuit model load means 2 reads a logical circuit model from a logical circuit model file 1 to load a logical circuit model table 3 and a control is transferred to a path detecting/ delay time calculating means 4. The means 4 takes out the path between the start and final points of the logical circuit model of the table 3 and calculates a delay time to store the same in a detected path memory means 7 and, when the path of the logical circuit model of the table 3 is not entirely detected at that point of time, control is transferred to a control value comparing means 6. The means 6 compares the delay time stored in the means 7 with a limit value 5 and, when said delay time is a contravention path, control is transferred to a redundant path judge means 9. The means 9 judges whether the contravention path is a redundant path an effective path using a route activating method; when said path is the effective path (error path), an error path display means 8 is started to output said path as error path display 10.

Previous Doc Next Doc Go to Doc#